



Intel™ 82430FX PCIset Level II  
**Cache Module Family**

**Features**

- Pin-compatible secondary cache module family that adheres to the Intel COAST 1.1 specification,
- Asynchronous (CYM74A430) or synchronous (CYM74S430, CYM74S431) configurations with presence and configuration detect pins
- Ideal for Intel P54C-based systems with the 82430FX (Triton) chip set
- Operates at 50, 60, and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V compatible inputs/outputs

**Functional Description**

This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chip set.

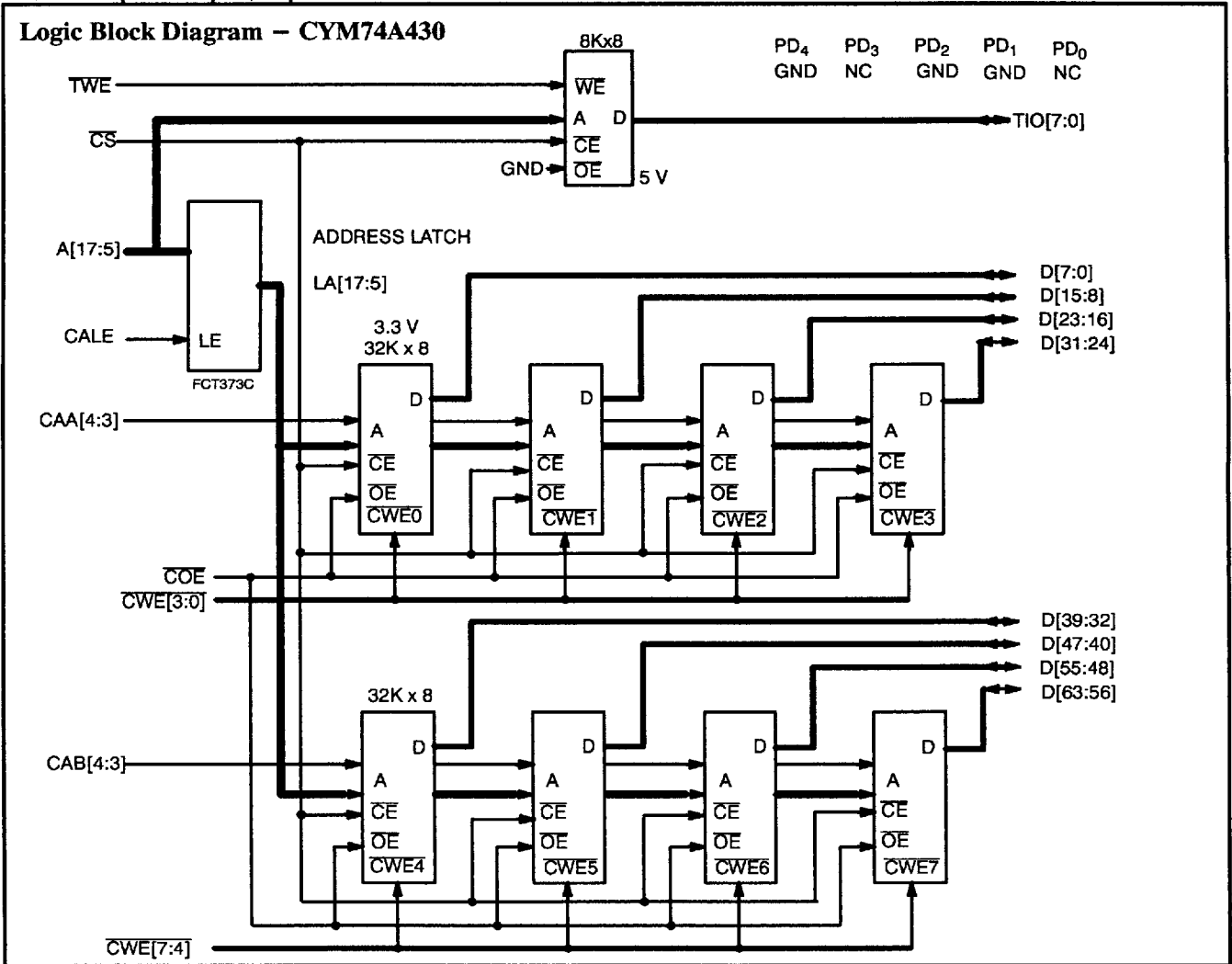
CYM74A430 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution. The CYM74A430 is organized as 32K by 64 data with an 8Kx8 tag that supports 3-2-2-2 read and 4-2-2-2 writes at 66 MHz.

The CYM74S430 and CYM74S431 are synchronous cache modules that provide 3-1-1-1 performance at 66 MHz. The CYM74S430 is a 256-Kbyte cache module organized as 32Kx64 with an 8Kx8 tag. The

CYM74S431 is a 512-Kbyte cache module organized as 64Kx64 with a 16Kx8 tag.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.



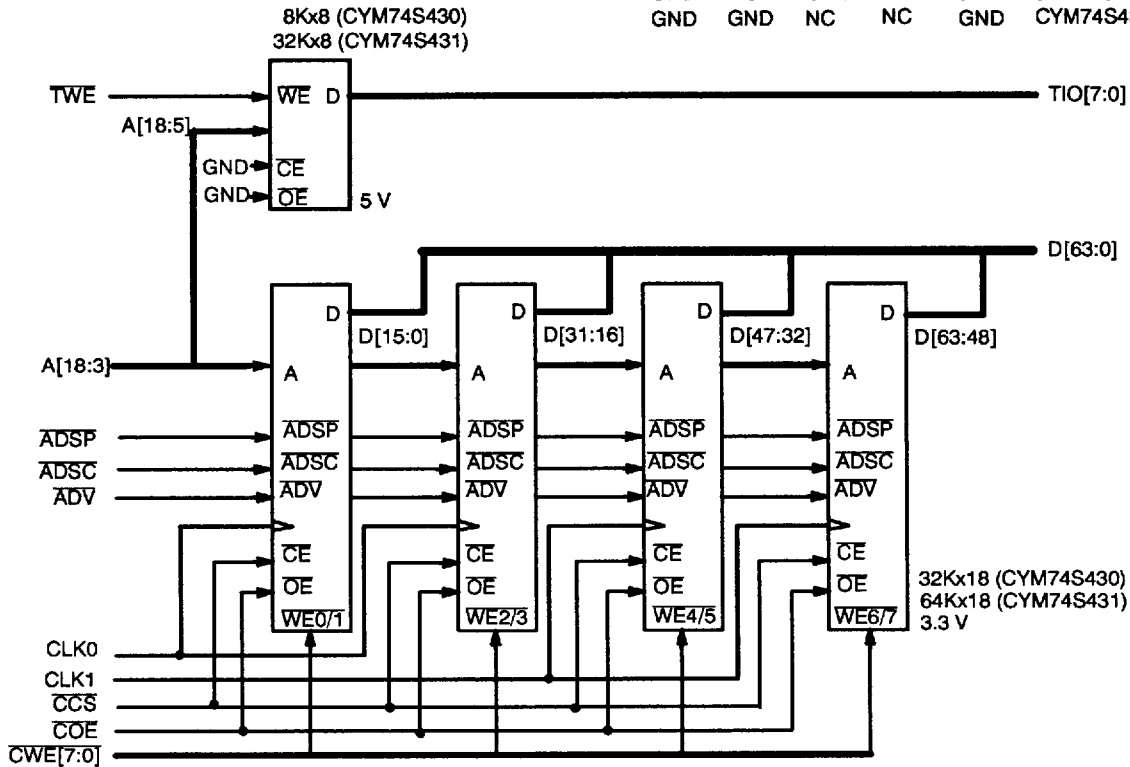
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**Logic Block Diagram – CYM74S430/CYM74S431**
**Notes:**

A18 is not used by CYM74S430

 DP pins are pulled high through 10 K $\Omega$ 

PD <sub>4</sub>	PD <sub>3</sub>	PD <sub>2</sub>	PD <sub>1</sub>	PD <sub>0</sub>	
GND	NC	GND	NC	GND	CYM74S430
GND	GND	NC	NC	GND	CYM74S431


**Selection Guide**

	74A430-50	74A430-60	74A430-66	74S430-50	74S430-60	74S430-66	74S431-50	74S431-60	74S431-66
Cache Size	256 KB			256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66	50	60	66
RAM Type	Async			Sync Burst			Sync Burst		
Data t <sub>AA</sub>	20 ns	17 ns	15 ns						
Data t <sub>CDV</sub>				13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t <sub>AA</sub>	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns



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Pin Configuration

Dual Read-Out SIMM (DIMM)

Top View

GND	81	1	GND
TIO <sub>1</sub>	82	2	TIO <sub>0</sub>
TIO <sub>7</sub>	83	3	TIO <sub>2</sub>
TIO <sub>5</sub>	84	4	TIO <sub>6</sub>
TIO <sub>3</sub>	85	5	TIO <sub>4</sub>
RSVD	86	6	RSVD
V <sub>CC</sub>	87	7	V <sub>CCQ</sub>
RSVD	88	8	TWE
(CYM74S43x) $\overline{ADV}$ /(CYM74A430)	89	9	CAA <sub>3</sub> (CYM74A430)/ $\overline{ADSC}$ (CYM74S43x)
GND	90	10	GND
COE	91	11	CWE <sub>4</sub>
CWE <sub>5</sub>	92	12	CWE <sub>6</sub>
CWE <sub>7</sub>	93	13	CWE <sub>0</sub>
CWE <sub>1</sub>	94	14	CWE <sub>2</sub>
V <sub>CC</sub>	95	15	V <sub>CCQ</sub>
(CYM74S43x) NC/(CYM74A430)	96	16	CAB <sub>4</sub> (CYM74A430)/ $\overline{CCS}$ (CYM74S43x)
(CYM74S43x) NC/(CYM74A430)	97	17	NC (CWE)
(CYM74S43x) NC/(CYM74A430)	98	18	NC (BWE)
GND	99	19	GND
RSVD	100	20	A <sub>3</sub>
A <sub>4</sub>	101	21	A <sub>7</sub>
A <sub>6</sub>	102	22	A <sub>5</sub>
A <sub>8</sub>	103	23	A <sub>11</sub>
A <sub>10</sub>	104	24	A <sub>16</sub>
V <sub>CC</sub>	105	25	V <sub>CCQ</sub>
A <sub>17</sub>	106	26	A <sub>18</sub>
GND	107	27	GND
A <sub>9</sub>	108	28	A <sub>12</sub>
A <sub>14</sub>	109	29	A <sub>13</sub>
A <sub>15</sub>	110	30	NC (CYM74A430)/ADSP (CYM74S43x)
RSVD	111	31	$\overline{CS}$ (CYM74A430)/NC (CYM74S43x)
PD <sub>0</sub>	112	32	NC (ECS2)
PD <sub>2</sub>	113	33	PD <sub>1</sub>
PD <sub>4</sub>	114	34	PD <sub>3</sub>
GND	115	35	GND
(CYM74S43x) CLK <sub>0</sub> /(CYM74A430)	116	36	NC (CYM74A430)/CLK <sub>1</sub> (CYM74S43x)
GND	117	37	GND
D <sub>63</sub>	118	38	D <sub>62</sub>
V <sub>CC</sub>	119	39	V <sub>CCQ</sub>
D <sub>61</sub>	120	40	D <sub>60</sub>
D <sub>59</sub>	121	41	D <sub>58</sub>
D <sub>57</sub>	122	42	D <sub>56</sub>
GND	123	43	GND
D <sub>55</sub>	124	44	D <sub>54</sub>
D <sub>53</sub>	125	45	D <sub>52</sub>
D <sub>51</sub>	126	46	D <sub>50</sub>
D <sub>49</sub>	127	47	D <sub>48</sub>
GND	128	48	GND
D <sub>47</sub>	129	49	D <sub>46</sub>
D <sub>45</sub>	130	50	D <sub>44</sub>
D <sub>43</sub>	131	51	D <sub>42</sub>
V <sub>CC</sub>	132	52	V <sub>CCQ</sub>
D <sub>41</sub>	133	53	D <sub>40</sub>
D <sub>39</sub>	134	54	D <sub>38</sub>
D <sub>37</sub>	135	55	D <sub>36</sub>
GND	136	56	GND
D <sub>35</sub>	137	57	D <sub>34</sub>
D <sub>33</sub>	138	58	D <sub>32</sub>
D <sub>31</sub>	139	59	D <sub>30</sub>
V <sub>CC</sub>	140	60	V <sub>CCQ</sub>
D <sub>29</sub>	141	61	D <sub>28</sub>
D <sub>27</sub>	142	62	D <sub>26</sub>
D <sub>25</sub>	143	63	D <sub>24</sub>
GND	144	64	GND
D <sub>23</sub>	145	65	D <sub>22</sub>
D <sub>21</sub>	146	66	D <sub>20</sub>
D <sub>19</sub>	147	67	D <sub>18</sub>
V <sub>CC</sub>	148	68	V <sub>CCQ</sub>
D <sub>17</sub>	149	69	D <sub>16</sub>
D <sub>15</sub>	150	70	D <sub>14</sub>
D <sub>13</sub>	151	71	D <sub>12</sub>
GND	152	72	GND
D <sub>11</sub>	153	73	D <sub>10</sub>
D <sub>9</sub>	154	74	D <sub>8</sub>
D <sub>7</sub>	155	75	D <sub>6</sub>
V <sub>CC</sub>	156	76	V <sub>CCQ</sub>
D <sub>5</sub>	157	77	D <sub>4</sub>
D <sub>3</sub>	158	78	D <sub>2</sub>
D <sub>1</sub>	159	79	D <sub>0</sub>
GND	160	80	GND



## Pin Definitions

Signal Name	Description
V <sub>CC</sub>	5V Supply
V <sub>CC0</sub>	3.3V Supply
GND	Ground
A[18:3]	Addresses from processor
CAA[4:3]	Lower two address bits for bank 0 of CYM74A430
CAB[4:3]	Lower two address bits for bank 1 of CYM74A430
$\overline{CS}$	Chip Select (CYM74A430 only)
CCS	Chip Select for CYM74S430 and CYM74S431
$\overline{COE}$	Output Enable
$\overline{CWE}$ [7:0]	Byte Write Enables
CALE	Latch Enable – CYM74A430 only
PD <sub>0</sub> –PD <sub>4</sub>	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
$\overline{TWE}$	Tag Written Enable signal
ASDP	Processor Address Strobe for CYM74S430 and CYM74S431
$\overline{ADSC}$	Cache Controller Address Strobe for CYM74S430 and CYM74S431
ADV	Burst Address Advance for CYM74S430 and CYM74S431
CLK[1:0]	Clock signals for CYM74S430 and CYM74S431
NC	Signal not connected on module.
RSVD	Reserved.

## Presence Detect Pins

	PD <sub>4</sub>	PD <sub>3</sub>	PD <sub>2</sub>	PD <sub>1</sub>	PD <sub>0</sub>
Asynchronous – CYM74A430	GND	NC	GND	GND	NC
Synchronous – CYM74S430	GND	NC	GND	NC	GND
Synchronous – CYM74S431	GND	GND	NC	NC	GND



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**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Ambient Temperature  
 with Power Applied .....  $-0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$   
 3.3V Supply Voltage to Ground Potential ....  $-0.5\text{V}$  to  $+4.6\text{V}$   
 5V Supply Voltage to Ground Potential .....  $-0.5\text{V}$  to  $+5.25\text{V}$   
 DC Voltage Applied to Outputs  
 in High Z State .....  $-0.5\text{V}$  to  $+4.6\text{V}$

DC Input Voltage .....  $-0.5\text{V}$  to  $+4.6\text{V}$   
 Output Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$ $3.3\text{V} \pm 5\%$

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CCQ</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min. I <sub>OH</sub> = -4 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min. I <sub>OL</sub> = 8 mA		0.4	V
I <sub>CC</sub> (74A430)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1500	mA
I <sub>CC</sub> (74S430)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1200	mA
I <sub>CC</sub> (74S431)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1200	mA

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A430PM-50	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM-50	PM28		Sync 256 KB	
	CYM74S431PM-50	PM28		Sync 512 KB	
60	CYM74A430PM-60	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM-60	PM28		Sync 256 KB	
	CYM74S431PM-60	PM28		Sync 512 KB	
66	CYM74A430PM-66	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM-66	PM28		Sync 256 KB	
	CYM74S431PM-66	PM28		Sync 512 KB	

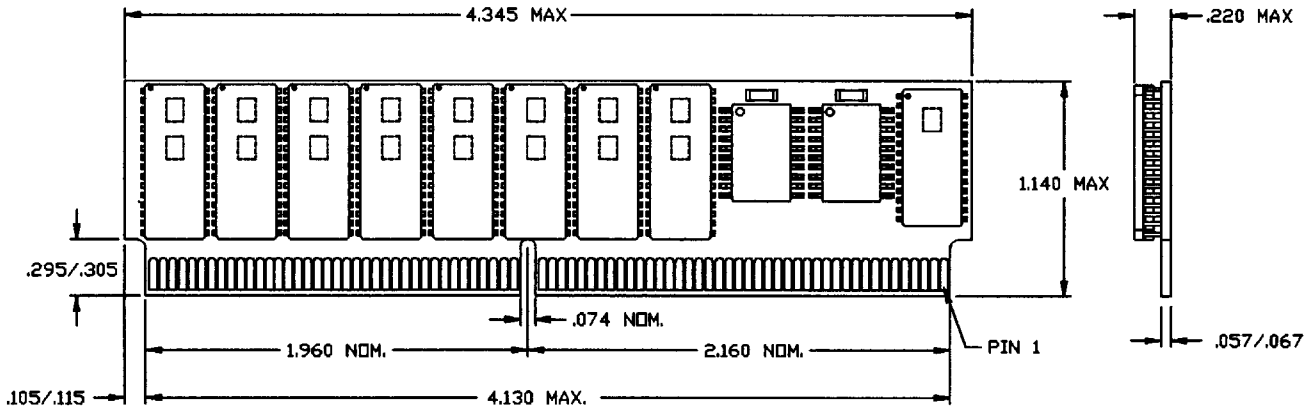
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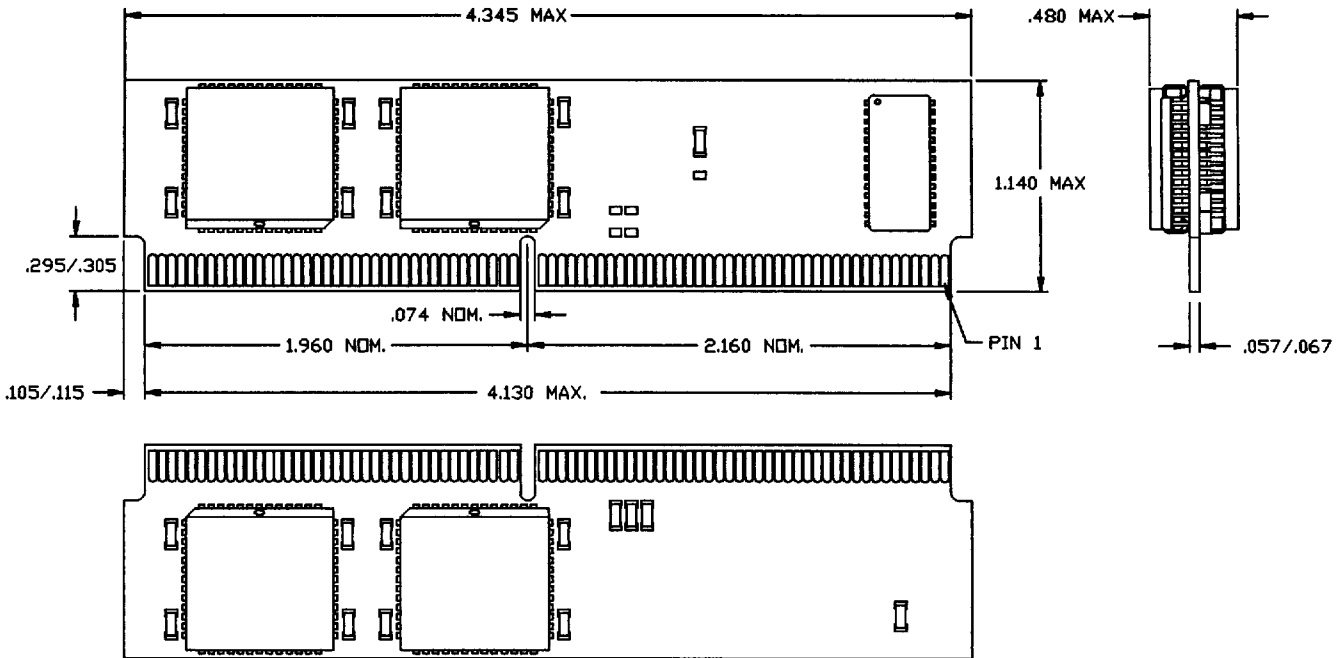
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Package Diagrams

160-Pin Dual Readout SIMM PM27



160-Pin Dual Readout SIMM PM28



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