CYPRESS

PRELIMINARY

CYM74A430
CYM74S430
CYM74S431

Intel™ 82430FX PCIset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family that adheres to the Intel COAST 1.1 specification,**
- **Asynchronous (CYM74A430) or synchronous (CYM74S430, CYM74S431) configurations with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the 82430FX (Triton) chip set**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V compatible inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chip set.

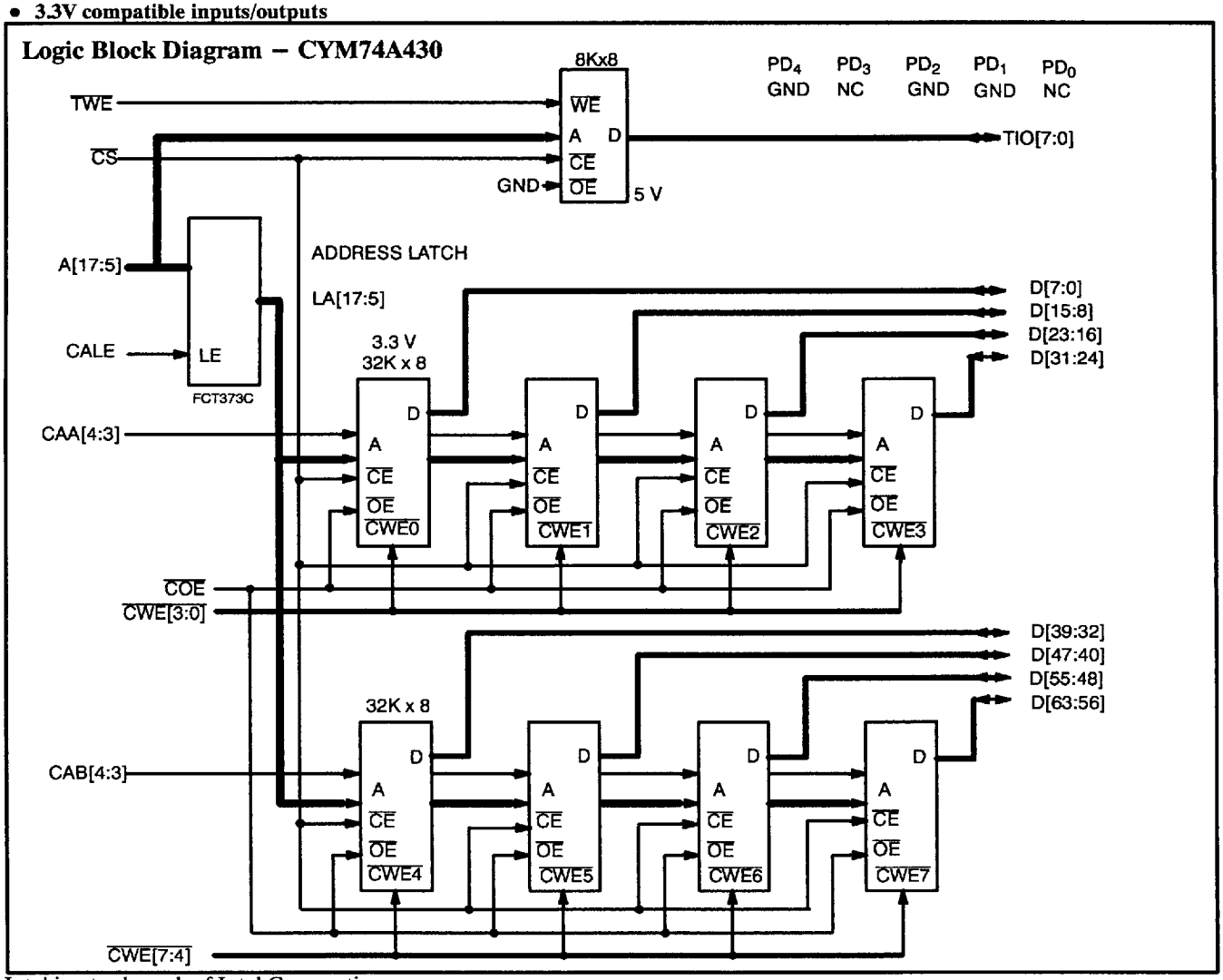
CYM74A430 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution. The CYM74A430 is organized as 32K by 64 data with an 8Kx8 tag that supports 3-2-2-2 read and 4-2-2-2 writes at 66 MHz.

The CYM74S430 and CYM74S431 are synchronous cache modules that provide 3-1-1-1 performance at 66 MHz. The CYM74S430 is a 256-Kbyte cache module organized as 32Kx64 with an 8Kx8 tag. The CYM74S431 is a 512-Kbyte cache module organized as 64Kx64 with a 16Kx8 tag.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

Logic Block Diagram – CYM74A430



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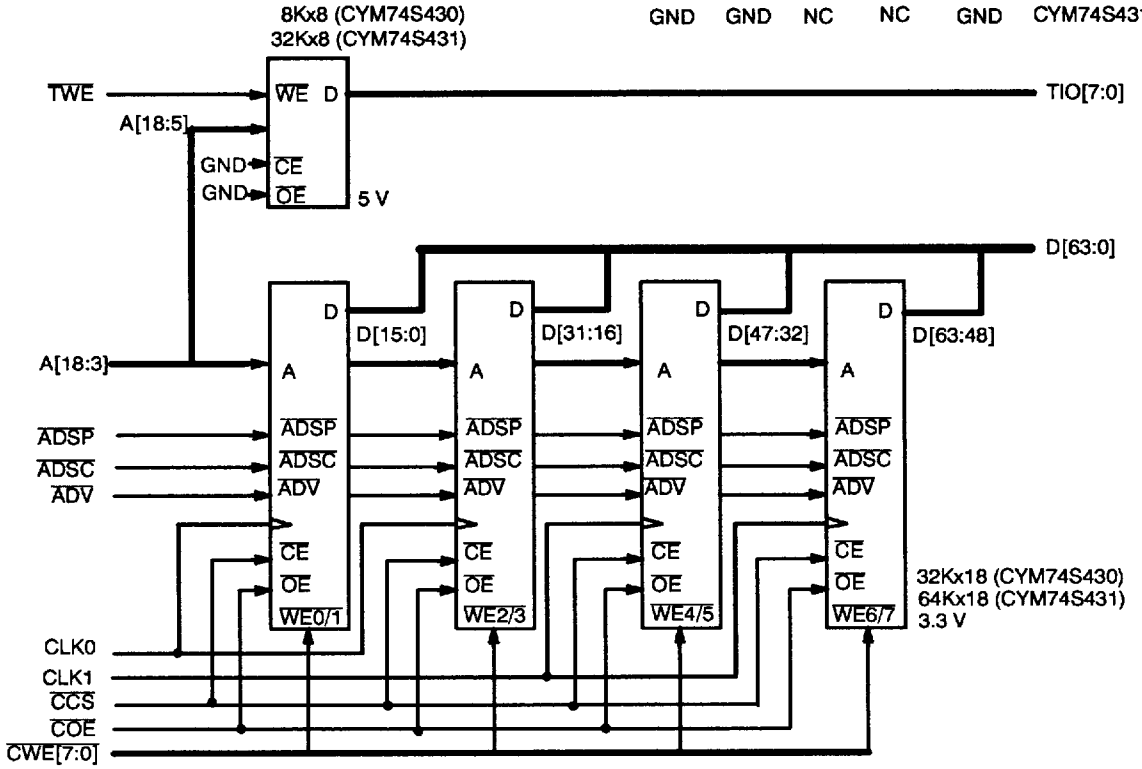
Logic Block Diagram – CYM74S430/CYM74S431

Notes:
A18 is not used by CYM74S430
DP pins are pulled high through 10 KΩ

PD_4	PD_3	PD_2	PD_1	PD_0	
GND	NC	GND	NC	GND	CYM74S430
GND	GND	NC	NC	GND	CYM74S431

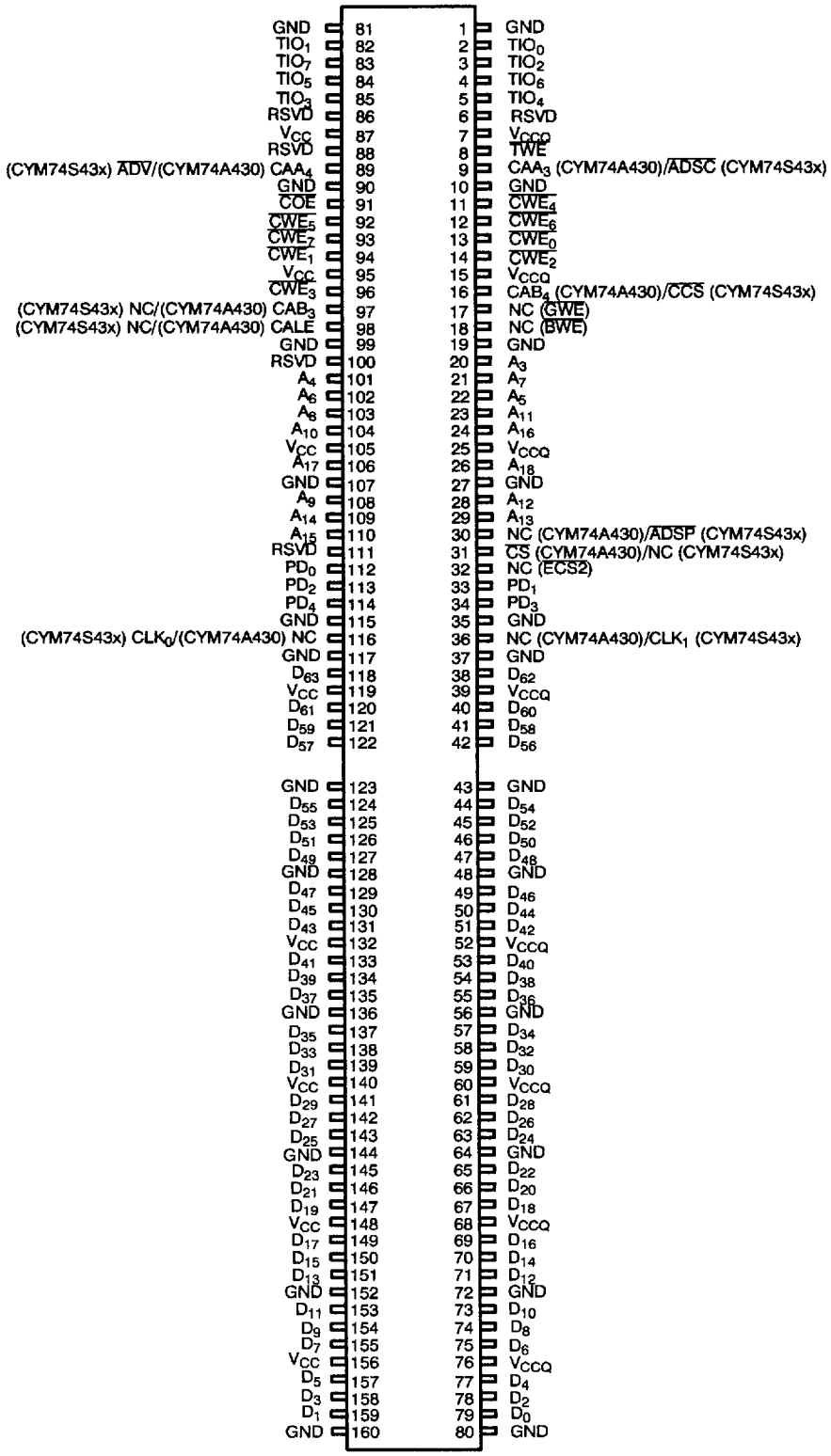


Selection Guide

	74A430–50	74A430–60	74A430–66	74S430–50	74S430–60	74S430–66	74S431–50	74S431–60	74S431–66
Cache Size	256 KB			256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66	50	60	66
RAM Type	Async			Sync Burst			Sync Burst		
Data t_{AA}	20 ns	17 ns	15 ns						
Data t_{CDV}				13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



Pin Definitions

Signal Name	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
A[18:3]	Addresses from processor
CAA[4:3]	Lower two address bits for bank 0 of CYM74A430
CAB[4:3]	Lower two address bits for bank 1 of CYM74A430
$\overline{CS}$	Chip Select (CYM74A430 only)
$\overline{CCS}$	Chip Select for CYM74S430 and CYM74S431
$\overline{COE}$	Output Enable
$\overline{CWE}$[7:0]	Byte Write Enables
CALE	Latch Enable – CYM74A430 only
PD_0–PD_4	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
$\overline{TWE}$	Tag Writen Enable signal
$\overline{ASDP}$	Processor Address Strobe for CYM74S430 and CYM74S431
$\overline{ADSC}$	Cache Controller Address Strobe for CYM74S430 and CYM74S431
$\overline{ADV}$	Burst Address Advance for CYM74S430 and CYM74S431
CLK[1:0]	Clock signals for CYM74S430 and CYM74S431
NC	Signal not connected on module.
RSVD	Reserved.

Presence Detect Pins

	PD_4	PD_3	PD_2	PD_1	PD_0
Asynchronous – CYM74A430	GND	NC	GND	GND	NC
Synchronous – CYM74S430	GND	NC	GND	NC	GND
Synchronous – CYM74S431	GND	GND	NC	NC	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74A430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74S430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200	mA
I_{CC} (74S431)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A430PM−50	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−50	PM28		Sync 256 KB	
	CYM74S431PM−50	PM28		Sync 512 KB	
60	CYM74A430PM−60	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−60	PM28		Sync 256 KB	
	CYM74S431PM−60	PM28		Sync 512 KB	
66	CYM74A430PM−66	PM27	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74S430PM−66	PM28		Sync 256 KB	
	CYM74S431PM−66	PM28		Sync 512 KB	

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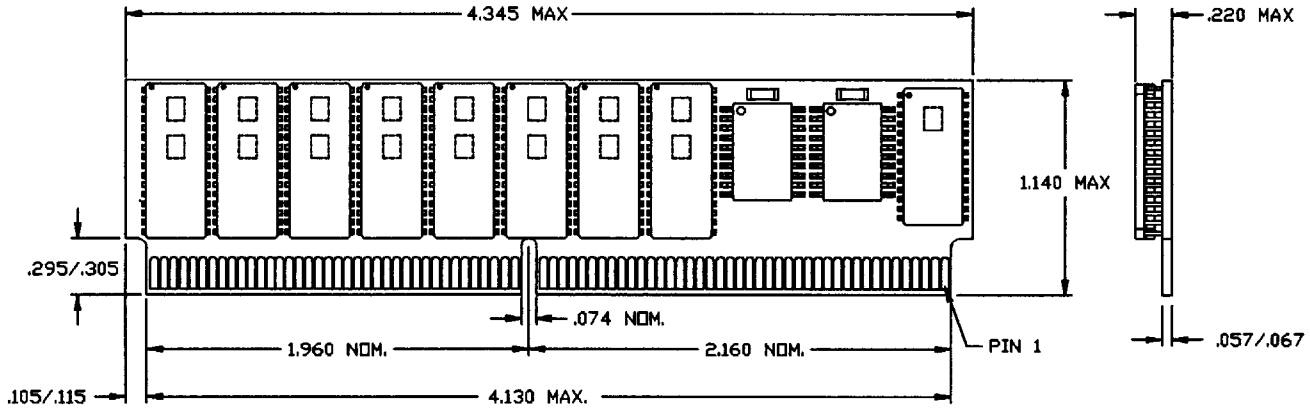
Package Diagrams

160-Pin Dual Readout SIMM PM27



160-Pin Dual Readout SIMM PM28